UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/870,253	05/30/2001	Jong-Hong Bae	29926/36988	8837

4743 7590 03/15/2004

MARSHALL, GERSTEIN & BORUN LLP
6300 SEARS TOWER
233 S. WACKER DRIVE
CHICAGO, IL 60606

EXAMINER	
KIK, PHALLAKA	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 03/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/870,253	Applicant(s) BAE ET AL.	
	Examiner Phallaka Kik	Art Unit 2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 November 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action responds to Applicant's amendment filed on 11/5/2003. Claims 1-3,5-9 are pending, wherein claim 4 has been cancelled and claims 11-3,5-7,9 have been amended. Claims 1-3,5-9 have been examined. However, Applicant's arguments are not persuasive; therefore, the previous Office Action is incorporated herein.

Priority

2. As indicated previously, receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Objections

3. **Claims 3,6-9** are objected to because of the following informalities:

As per **claim 3**, "claim 1" (line 1) should be --claim 2-- to provide proper antecedent basis for "the first set of multiplexers" (line 1), "the plurality of decoded output signals" (lines 4-5) and "the port data decoder" (lines 6).

As per **claim 6**, "the programs" (line 8) should be --the program--for proper antecedent basis since "program" (singular) (line 5) is being referred to; "MUC" (line 11) should be --MCU-- for proper antecedent basis; "the coded output signals" (line 13) should be --coded output signals-- for proper antecedent basis.

As per **claims 7-9**, the claims are objected to for incorporating the above errors into the respective claims by claim dependency.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. **Claims 1-3,5-9** are rejected under 35 U.S.C. 102(b) as being anticipated by **Butts et al.** (US Patent No. 5,796,623).

Butts et al. disclose an apparatus and method for performing computations, prototyping, execution, simulation using electrically reconfigurable gate arrays (ERCGA) logic chips (abstract).

As per **claims 1,2,6,8-9**, all of the elements of the claims are illustrated in Fig. 1, wherein the target board corresponds to one of the boards in the Realizer Hardware System (see col. 7, lines 44-46), the MCU corresponds to the Host Computer (see Figs. 49, 54-57 for interactions of the host computer to generate the necessary signals/commands/programs to configure/re-configure/analyze/simulate the circuit, i.e., I/O control means and means for receiving and providing, using the Realizer Hardware System), the storage blocks (or receiving means), including RAMS and register addresses and data are further described in col. 24, line 10 to col. 34, line 53, wherein the decoder and multiplexer associated with data and address accesses are further described in col. 27, line 26 to col. 28, line 6 (see also col. 33, lines 1-20); wherein the

multiplicity of I/O ports or pins associated with the communication means are part of the host interface (col. 7, lines 38-63; col. 8, lines 21-59).

As per **claim 3**, the multiplexers including a three-phase buffer (i.e., tri-state buffers) and a second or plurality of multiplexer(s) are further described in col. 33, lines 1-20.

As per **claims 5,7**, the particular interactions of the i/o ports (e.g., I/O control means) in conjunction with the multiplexers, RAM or register data and addresses, are further illustrated in Figs. 24-27, 32-33.

Remarks

6. The objections of **claims 3,5-9** due to the previously noted informalities are withdrawn as being corrected by Applicant's amendment filed on 11/5/2003. However, as noted above, claims 3,6-9 are still objected to due to minor informalities introduced by Applicant's amendment to the claims.

7. As per **claims 1-3,5-9**, Applicant argued that **Butts et al.** failed to anticipate Applicant's claimed invention because the MCU as claimed is not contained in a single chip with the I/O block, the SFR block or the like due to the requirement of the pin connections in the independent claims 1 and 6; thus one can test a plurality of circuits designed in accordance with specific functions separately without simultaneously testing the external I/O blocks and external pins of the MCU. The Examiner is not persuaded. First of all, Applicant's claims do not recite the limitation that the MCU do not contain on a single chip as asserted by Applicant since an integrated chip could also include the particular I/O pin connections as claimed. Second, the system of **Butts et al.** provides

for all of the elements of the claims, regardless whether it is built on a single chip or not, since the particular I/O pins and interactions thereof are equivalent to Applicant's claimed invention. Third, since the particular configuration of the hardware circuit(s) depends on the circuit design to be tested, emulated and/or simulated, and the hardware circuit(s) is (are) equipped with the particular I/O ports or pins, the specific functions of the circuit design can be separately tested (see col. 8, lines 29-46).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Therefore, Applicant is requested to consider them carefully in response to this Office Action.

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phallaka Kik whose telephone number is 571-272-1895. The examiner can normally be reached on Flexitime.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any response to this action should be mailed to:

Commissioner for Patents

P. O. Box 1450

Alexandria, VA 22313-1450

or faxed to:

703-872-9318 (for Before-Final) and 703-872-9319 (for After-Final) for formal communications intended for entry,

Or:

(571) 273-1895 (for informal or draft communications, please label

"PROPOSED" or "DRAFT" and let the examiner know prior to faxing).

11. **Applicant should note that effective May 1, 2003, the United States Patent and Trademark Office has a new Commissioner for Patents address for transitioning to the new Office location in Alexandria, VA, wherein correspondence in patent-related matters to organizations reporting to the Commissioner for Patents must now be addressed to:**

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

PK
March 7, 2004

MATTHEW SMITH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800